J5DY

375.00 201 A

07628440

501

OPTIMIZED PIEZOELECTRIC RESONATOR-BASED NETWORKS AND ASSOCIATED METHOD

BACKGROUND OF THE INVENTION

This invention relates to piezoelectric resonators and, specifically, to a method for optimizing the topology of a piezoelectric resonator-based network so that it may be implemented, either in monolithic or discrete form, ~~without the need for additional interconnects to complete connections~~ B1.

A typical prior piezoelectric resonator comprises a wafer of piezoelectric material such as quartz or ceramic material provided with electrodes mounted on the wafer's opposing lateral surfaces. Upon application of an alternating voltage to the electrodes, the piezoelectric material is driven electrically in a predetermined vibrational mode, for example, thickness shear, thickness extensional, etc., depending on the orientation or polarization of the piezoelectric material. The resonant frequency of the resonator is dependent on the overall wafer and electrode thickness and increases with a decrease in thickness. At high frequencies very thin wafers, plates, or films are required in order to have a half wavelength established across the thickness. ~~Through~~ B2 different network configurations or with additional circuitry, such resonators can be combined to form filters or oscillators.

Prior resonators have been constructed in a number of ways. The most prevalent method is to construct

individual resonators, mount and package them and then connect the packaged resonators into various circuit configurations. In an effort to reduce the overall circuit size, more than one resonator may be fabricated on a single plate of piezoelectric material and then interconnected on the plate to form a circuit. As shown in U.S. Pat. No. 3,222,622, the wafer may be cut to a desired thickness and the electrodes then mounted on opposing surfaces of the wafer. Another approach exemplified in U.S. Pat. No. 3,590,287 is to utilize a deposition process. The electrodes and piezoelectric material are deposited as metalization layers and a thin film, respectively, on a substrate such as a quartz wafer.

Although satisfactory resonators can be constructed with these techniques, they have their drawbacks. In both cases the two opposing electrodes of the resonator are on opposing lateral surfaces of the piezoelectric material and not coplanar. These electrodes, which connect the resonator to other circuitry such as integrated circuits or discrete components, may not be favorably positioned for making such connections. This is especially true if the piezoelectric material rests on a substrate and the electrode between the two materials is thus buried. Connecting the buried electrode to a discrete component such as a resistor is quite difficult. B3

One solution suggested in U.S. Patent No. 3,222,622 is to provide a nonplanar conductive interconnect between a poorly positioned electrode and an additional electrode mounted in a more favorable position. Connections to other circuitry may then be made from the additional electrode. As shown therein, an interconnect in the form of a discrete wire is added to a pi-network to connect an electrode mounted on the lower surface of the piezoelectric material to an electrode mounted on the upper surface of the material. The interconnect extends around the edge of the material, and is added as an additional step in the process of constructing the resonator.

An alternative solution might be to fabricate a via interconnect that extends through the piezoelectric material to make the desired connection. The interconnect is fabricated with additional steps in the process of constructing the resonator.

Neither of these solutions, however, is conducive to high volume, low cost manufacturing. Both add additional, costly steps to the manufacturing process. ~~Consequently, individually packaged resonators have remained popular despite the area and effort they require to construct multiple resonator networks.~~

Cl

P

SUMMARY OF THE INVENTION

Therefore, an object of the invention is to provide a method for optimizing the topology of a piezoelectric resonator-based network which overcomes the drawbacks of the prior art.

Another object of the invention is to provide piezoelectric resonator-based networks in which electrodes may be selectively placed on the piezoelectric material to provide desired connections to other circuitry without the need for additional, nonplanar interconnects.

In accordance with these objects, the method of the invention comprises decomposing an original resonator within a network into a pair of serially connected resonators which share a common electrode. The composite characteristics of the serial connected resonators are chosen to match the characteristics of the original resonator. By such decomposition, an additional electrode is added to the network and is placed on the piezoelectric material surface opposing the surface to which is mounted the shared electrode for making a desired connection to other circuitry. The method does not require a nonplanar interconnect for connecting an electrode on one surface of the piezoelectric material to circuitry present at the opposing surface. The invention thereby eliminates the difficulty of providing access to electrodes of the resonator network for connection to other circuitry. Ins. B6 KBa

S

The invention is applicable to monolithic resonator circuits as well as to discrete resonator circuits.

The foregoing and other objects, features, and advantages of the invention will become more apparent from the following detailed description of several preferred embodiments which proceeds with reference to the following drawings.

DR, Cl

BRIEF DESCRIPTION OF THE DRAWINGS

P

FIG. 1 is a schematic diagram of an electrical circuit that includes a piezoelectric resonator.

Ins. B7

FIG. ~~2A is a~~ B7 cross sectional view of a discrete embodiment of the resonator represented in FIG. 1.

Ins B8

FIG. ~~2B is a~~ B8 cross sectional views of a second embodiment of the resonator represented in FIG. 1 including a full substrate supporting the piezoelectric material.

Ins B9

~~FIG. 2C is a~~ B9 cross sectional views of a third embodiment of the resonator represented in FIG. 1 including a partial substrate supporting the piezoelectric material.

FIG. 3 is a schematic diagram of an equivalent resonator formed by decomposing the original resonator into a pair of series connected resonators.

6

Ins. B10

Ins. B11

~~FIG. 4 is a~~ B10 cross sectional views of an implementation of the series connected resonators of FIG. 3. B11

14 FIGS. 5A-D illustrate the process for fabricating the series connected resonators of FIG. 4.

FIG. 6 is a schematic diagram of an electrical circuit that includes a T network comprising several piezoelectric resonators and/or shunt elements.

Ins B12

~~FIG. 7 is a~~ B12 cross sectional views of a monolithic implementation of the T network represented in FIG. 6

FIG. 8 is a schematic diagram of an equivalent T network formed by decomposing a resonator in the T network into a pair of series connected resonators.

Ins B13

~~FIG. 9 is a~~ B13 cross sectional views of an implementation of the T network represented in FIG. 8.

14 FIGS. 10A-D illustrate the process for fabricating the T network of FIG. 9.

FIG. 11 is a schematic diagram of an electrical circuit that includes a pi network comprising piezoelectric resonators.

B FIG. 12 is a ~~cross sectional~~ perspective view of a monolithic implementation of the pi network represented in FIG. 11.

FIG. 13 is a schematic diagram of an equivalent pi network formed by decomposing each resonator of the network into a pair of series connected resonators.

B FIG. 14 is a ~~cross sectional~~ perspective view of an implementation of the pi network represented in FIG. 13.

7

14

FIGS. 15A-D illustrate the process for fabricating the pi network represented in FIG. 14.

FIG. 16 is a schematic diagram of an electrical circuit that includes an L network comprising piezoelectric resonators and shunt elements.

Ins. B14 C1

~~FIG. 17 is a cross sectional view~~ ~~B14~~ C1 of a monolithic implementation of the L network represented in FIG. 16.

FIG. 18 is schematic diagram of an equivalent L network formed by decomposing each of its resonators into a pair of series connected resonators.

Ins. B15 C2

~~FIG. 19 is a cross sectional view~~ ~~B15~~ C2 s of an implementation of the L network represented in FIG. 18.

14

FIGS. 20A-D illustrate the process for fabricating the L network of FIG. 19.

FIG. 21 is a schematic diagram of an electrical circuit that includes a ladder network comprising piezoelectric resonators and shunt elements.

Ins. B16 C3

~~FIG. 22 is a cross sectional view~~ ~~B16~~ C3 s of a monolithic implementation of the ladder network represented in FIG. 21.

FIG. 23 is a schematic diagram of an equivalent ladder network formed by decomposing a resonator of the network into a pair of series connected resonators.

Ins. B17 C4

~~FIG. 24 is a cross sectional view~~ ~~B17~~ C4 s of an implementation of the ladder network represented in FIG. 23.

8

FIG. 25 illustrates the process for fabricating ~~the~~ ladder network ~~of FIG~~. 24.

Insert B19

DESCRIPTION OF PREFERRED EMBODIMENTS

Referring now to FIG. 1, there is shown a schematic diagram of an electrical circuit that includes a piezoelectric resonator X1. Resonator X1 is of conventional design and includes a pair of electrodes M1 and M2 mounted on opposing surfaces of piezoelectric material 30. The resonator X1 is shown connected within an electrical circuit that includes a voltage source V_g in series with a generator impedance represented by resistor R_g. The resistor R_g is connected to the first electrode M1 of resonator X1. The second electrode M2 is connected to a load impedance represented by resistor R_1, which in turn is also connected to the voltage source V_g to complete the circuit. Resonator X1 in this circuit is a filter, with electrode M1 receiving an input signal and electrode M2 providing an output signal. As a filter, resonator X1 passes electrical signals with the same frequency as its piezoelectric material's series resonant frequency and attenuates or suppresses signals of other frequencies.

FIGS. 2A-C show different possible embodiments (not to scale) of the resonator X1 based on the circuit topology of FIG. 1. ~~FIG. 2A illustrates~~ B20 a bulk crystal resonator X1 comprising overlapping, opposing electrodes

9

M1 and M2 mounted on opposing surfaces of the piezoelectric material 30. To construct the resonator using known techniques, the crystal material is placed in a vacuum chamber and the metal for electrodes M1 and M2 is introduced as a vapor that deposits on the material's surfaces 42 and 44. The metal is then etched to form the desired electrodes. Resonators of this type are typically driven at their fundamental frequency. The portion of the embodiment between the dashed lines in FIG. 2A.2 forms the actual resonator X1. The portion 38 of electrode M1 outside the dashed lines forms a lead for interconnecting the resonator to other circuit elements such as resistor R_g. Similarly, the portion 40 of electrode M2 outside the dashed lines forms a lead for interconnecting the resonator to other circuit elements such as resistor R_1.

B

H

H

Ins. B21

Ins. B22

~~FIG. 2B shows~~ B21 a second embodiment of the resonator X1. Electrode M2 is deposited as a metal layer on a supporting substrate 32 such as silicon. B22 Deposited on top of layer M2 is a film of piezoelectric material 30. To complete the resonator X1 the metal layer M1 is deposited on top of the piezoelectric material 30. This embodiment may be used, for example, where it is desirable to place the resonator on a semiconductor wafer for interconnection to portions of adjacent integrated circuits. As is known in the art, the supporting substrate underneath the actual resonator X1 changes the electrical characteristics of the resonator from that of

10

FIG. 2A. The resonator of FIG. 2B is an overmoded resonator and is operated at high harmonics of the fundamental frequency.

INS. B23

~~FIG. 2C shows~~ B23 a third embodiment of the resonator X1 in which a selected part of the substrate 32 directly below the resonator has been removed. The remaining substrate has no effect on the electrical characteristics of the resonator. The resonator X1 in FIG. 2C can thus have the same electrical characteristics as the resonator X1 in FIG. 2A, and ~~is~~ may be constructed on a semiconductor wafer for interconnection to other circuitry on the substrate.

B

INS. B24

For the sake of simplicity, the present invention and prior art will be further described only with respect to resonators of a type such as shown in ~~FIG. 2C~~ B24. It should be understood, however, that the invention is also equally applicable to other types of resonators such as those shown in FIGS. 2A and 2B.

14

A drawback of the conventional topology of FIG. 1 and resultant embodiments of FIGS. 2A-C is the consequent nonplanar locations of the electrodes M1 and M2. The lead 40 of electrode M2, for example, is mounted to the lower surface of the piezoelectric material 30 and, if substrate 32 is present, buried between the substrate and piezoelectric material 30. To connect lead 40 to a discrete component such as resistor R_1 requires a bonding pad on the upper surface 42 of material 30 and either (1) a discrete nonplanar interconnect from the electrode M2

H B

around the edge of the piezoelectric material (as in U.S. Patent No. 3,222,622) or (2) a via interconnect through the material 30 to its upper surface. If, on the other hand, resistors R_g and R_1 are implemented in monolithic form on substrate 32, it may be desirable to connect to resistor R_g on the substrate 32 at the lower surface 44 of the material 30. This connection would require a interconnect from electrode M1 to the lower surface.

Regardless of where connections are desired, both connecting options are poor. A discrete nonplanar interconnect is too costly to design into a monolithic implementation. B25 A via interconnect requires forming a high definition hole in the piezoelectric material 30 and depositing conducting material into the hole to electrically connect an electrode to the opposing material surface. In typical piezoelectric resonators, extremely high height-to-width ratios are encountered which affect the reliability of such internal interconnects. Reducing the ratio, however, requires that the width of the via be increased. This in turn may unacceptably increase the lateral area required for the via. Moreover, forming the via interconnect would require additional fabrication processing steps. B26

Insert B27

The present invention provides a method of optimizing the topology of a piezoelectric resonator-based network so that nonplanar interconnects are not required for making such connections. The method, which

is applicable to the single resonator of FIG. 1 as well as to multiple resonator networks to be discussed, places additional electrodes where they are desired and provides a resonator network with electrical characteristics equivalent to the characteristics of the original resonator network.

FIG. 3 is a schematic diagram of a resonator equivalent to the resonator of FIG. 1 in which the topology is optimized for placing an additional electrode. The optimized network is formed by decomposing resonator X1 into a pair of series connected resonators X11 and X12. This decomposition in the present embodiment comprises locating a resonator in the network, such as X1, and replacing it with two series connected resonators X11 and X12 which are connected only to each other at a shared electrode M2. Electrode M2 is referred to as a floating electrode since it does not connect the resonators to other circuitry. Electrodes M1 and M3, on the other hand, are referred to as connecting electrodes since they connect the network to other circuitry, such as resistors R_g and R_l. The two series resonators X11 and X12 are designed to have composite characteristics that match those of the resonator X1 to preserve the original characteristics of the resonator. From a functional point of view, the resonators of FIG. 3 are equivalent to the resonator of FIG. 1, but an additional electrode M3 has

been added which replaces electrode M2 as a connecting electrode to other circuitry.

Ins. B

The difference between the conventional and new circuit topologies can be seen in the ~~cross sectional~~ perspective views of the implementation of the equivalent circuit in ~~FIG. 4~~ 1B28. Whereas the electrodes that connect to other circuitry were on opposing surfaces of piezoelectric material 30 in 14 FIGS. 2A-C, they are now on the same surface in FIG. 4 because of the addition of the third electrode M3. Electrodes M1 and M3 now form such a pair of planar connecting electrodes mounted to surface 42 of the piezoelectric material 30. Electrode M2, which is shared by resonators X11 and X12, is mounted to the opposing surface 44. Electrode M1 and M3 are mounted in overlapping relation to electrode M2 to create two series connected resonators that are connected only to each other at electrode M2. Electrode M2 is thus a floating electrode that does not connect to other circuitry. By decomposing the resonator X1 into the series connected resonators X11 and X12, the third electrode M3 is added on a surface opposing the surface on which the shared electrode M2 resides. This arrangement allows the network H to connect to resistors R_g and R_l through leads 38 of electrode M1 and lead 46 of electrode M3. If desired, electrodes M1 and M3 could as easily be placed on the H lower surface 44 (if R_g and R_l were substrate-based

14

resistors) by reversing the implementation's fabrication steps.

The method is not limited to placing connecting electrodes on the same surface of the piezoelectric material, but may be employed for placing them on opposing surfaces as well. This may occur, as will be seen, where a connection to an adjacent integrated circuit is desired at the lower surface 44 as well as a connection to a discrete component at the upper surface 42.

The method for optimizing the circuit topology therefore comprises the following steps. First an electrical resonator in the network is decomposed into a pair of series connected resonators to add an additional electrode to the network, the resonators sharing a common electrode. The composite characteristics of the series connected resonators are matched to those of the original resonator to preserve the original characteristics of the network. In the implementation of FIG. 4, this matching is done by changing the overlapping areas of the electrodes M1,M2 and M3,M2 so that the bulk capacitance of each series connected resonator X11, X12 is double the original bulk capacitance of resonator X1:

PSP IB

$$C_{X11} = C_{X12} = 2C_{X1}$$

RS

The additional electrode is then placed on a surface of the piezoelectric material 30 opposing the surface to which the shared electrode is mounted for making the desired connection. B29

Ins B29

15

P 14

FIGS. 5A-D illustrate the process for fabricating the series connected resonators of FIG. 3 /01 on a substrate 32. FIG. 5A shows the first layer metalizations that form electrode M2 ~~electrodes M1 and M3.~~ FIG. 5B shows the deposition of the piezoelectric material 30. FIG. 5C shows a second layer metalization that forms ~~electrode M2~~ D30. FIG 5D is a schematic view showing the relative locations of resonators X11 and X12 within the implementation.

The described method may be applied to any resonator network for the purpose of placing an additional connecting electrode on a desired surface of the piezoelectric material 30. In the embodiment described above, the additional connecting electrode was placed on the same surface as the connecting electrode M1 was placed. It may be desirable in some cases, however, to place an additional connecting electrode on the surface opposing the other connecting electrode so that the connections to other circuitry are on opposing surfaces of the piezoelectric material 30. ~~For example, a resonator may connect at its input to a buried metal layer of a transistor and at its output to a discrete component that must be bonded to an electrode on the upper surface 42 of the resonator~~.

FIG. 6 is a schematic diagram of an electrical circuit that includes a T resonator network. The T network comprises resonator X1, a series resonator X2 and a shunt element such as piezoelectric resonator X3. All

16

of the resonators share a common electrode M2. Electrode M1 connects the T network via resonator X1 to other circuitry such as resistor R_g and electrode M3 connects the network via resonator X2 to other circuitry such as resistor R_1. Another electrode MG connects the network via resonator X3 to signal ground. Electrode M2 in this network is a floating electrode.

INS. B31

~~FIG. 7 is a cross section~~ B31 of an implementation of the T network based on the circuit topology of FIG. 6~~,~~ ~~taken at a point to omit electrode MG for clarity.~~ INS. B32 Electrodes ~~M1 and M3~~ B32 are mounted as a coplanar metal layers on supporting substrate 32. Deposited on top of these electrodes is the film of piezoelectric material 30. To complete resonators X1, X2 and X3, the metal layer~~s~~ M2 is ~~and MG are~~ deposited on the upper surface 42 of the piezoelectric material 30. The portions of the implementation between pairs ~~one pair~~ of dashed lines form~~s~~ the INS. B33 ~~resonator X1 and between the other pair of dashed lines~~ B33 INS. B34 ~~forms the resonator X2~~ B34. The portion 38 of electrode M1 outside resonator X1 forms a lead for interconnecting the resonator to other circuit elements such as resistor R_g. Similarly, the portion 46 of electrode M3 outside the dashed lines defining resonator X2 forms a lead for interconnecting the resonator to other circuit elements such as resistor R_1. Both electrodes M1 and M3 are buried between substrate 32 (not shown) and material 30.

17

If it is desired to make a connection to the network at the upper surface 42 of piezoelectric material 30, the method of the present invention is employed to optimize the network's topology for that purpose. FIG. 8 is a schematic diagram of an equivalent T network formed by decomposing resonator X2 into a pair of series connected resonators X21 and X22. Resonators X1 and X21 form a pair of series connected resonators sharing a first electrode M2. Resonator X3 is a shunt element that also connects to electrode M2 and to signal ground via electrode MG. A resonator X22 is series connected to resonator X21 at electrode M3. But unlike other electrodes within the T network, only the two resonators are connected at electrode M3. The additional resonator X22 adds an additional connecting electrode M4 to the T network. The composite characteristics of the series connected resonators are chosen to match the characteristics of resonator X2 which they replace so that the network's electrical characteristics remain unchanged.

INS. B35

~~FIG. 9 is a~~ B35 cross sectional view 5 of a monolithic implementation of the network of FIG. 8. With resonator X2 replaced with series connected resonators X21 and X22, the additional connecting electrode M4 is deposited on the upper material surface 42. Resonators X21 and X22 are formed by overlapping areas of electrodes M2, M3 and M4, as indicated by the dashed lines B36 defining the resonators. The portion of electrode M4 outside the dashed lines

INS. B36

18

defining resonator X22 forms a lead 64 on the upper surface 42 of piezoelectric material 30 for interconnecting the T network to other circuitry. With this additional electrode, electrode M1 may connect to an adjacent integrated circuit at lower surface 44 and electrode M4 may be bonded to a discrete component at upper surface 42.

14 B 8
Ins D2

FIGS. 10A-D illustrate the process for fabricating ~~the~~ an the implementation ~~of FIG. 9.~~ of similar to B2 FIG. 10A shows the first layer metalizations that form electrodes M1, M3 and MG. FIG. 10B shows the deposition of the piezoelectric material 30. FIG. 10C shows a second layer metalization that forms electrodes M2 and M4. FIG 10D is a schematic view showing the relative locations of resonators X1, X21, X22 and X3 within the implementation of the T network.

If desired, resonator X3 of FIG. 8 may be decomposed to produce a pair of series connected resonators as the shunt element. This decomposition would place signal ground on an opposing surface of material 30 from other electrodes X1 and X2 that connect the network to other circuitry.

The method of the invention covers other resonator networks as well. FIG. 11 shows the topology of a conventional pi network within a circuit. The network comprises several ~~series~~ connected resonators X1, X2 and X3. Electrode M1 is shared by resonators X1 and X2 and

B

19

provides a lead for interconnecting the network to other circuitry such as resistor R_g to receive an input for the network. Similarly, electrode M2 is shared by resonators ~~X2~~ X1 and X3 and provides a lead for interconnecting the network to other circuitry such as resistor R_1 to provide an output for the network. Electrodes MG1 and MG2 complete resonators X2 and X3, respectively, and are leads for interconnecting the network to signal ground. These electrodes, however, are on opposing surfaces of the piezoelectric material 30 because of the circuit topology.

FIG. 12 is a ~~cross sectional~~ perspective view of a monolithic implementation of the pi network of FIG. 11. ~~Electrode M1 is adjacent to the lower~~ B38 material surface ~~44~~ 42 B37 and ~~electrode~~ 44 B39 M2 is adjacent to the ~~upper~~ lower material surface ~~42~~. ~~Although~~ not visible in this view, it should be ~~understood~~ understood that electrode MG1 is also adjacent to the upper material surface 42, coplanar with electrode M2, and electrode MG2 is adjacent to the lower material surface 44, coplanar with electrode M1.

The topology of the circuit in FIG. 11 has a distinct disadvantage when implemented in either monolithic or discrete form. The electrodes MG1 and MG2 are on opposing surfaces of piezoelectric material 30, although they are both signal ground. To join them requires a nonplanar interconnect. If the two electrodes were on the same surface, however, they could be combined into a single electrode. If it is desired to connect

electrode M2 to other circuitry at the lower surface 44, then a nonplanar interconnect from electrode M2 to the lower surface is required.

These disadvantages are overcome by application of the present method to optimize the circuit's topology. FIG. 13 is a schematic diagram of an equivalent pi network formed according to the method by decomposing each resonator into a pair of series connected resonators. Resonator X1 is replaced with series connected resonators X11 and X12, adding an additional electrode M3. Resonator X2 is replaced with series connected resonators X21 and X22, adding an additional electrode M4. Resonator X3 is replaced with series connected resonators X31 and X32, adding an additional electrode M5. In each case, the composite characteristics of the series connected resonators are chosen to match the characteristics of the replaced resonator so that the pi network's electrical characteristics remain unchanged.

3

The replacement of resonators X2 and X3 is optional, depending only on the desired location of the signal ground electrode MG. An equivalent pi network that includes resonators X2 and X3 would comprise a first pair of resonators such as X11 and X2 sharing a first electrode for connection to other circuitry. A second pair of resonators such as X12 and X3 would share a second electrode for connection to other circuitry. A series connected pair of resonators would then be formed

24

comprising resonators X11 and X12 and a third electrode such as electrode M2. The series connected pair of resonators would be the only connections to electrode M2.

FIG. 14 is a Perspective ~~cross sectional~~ view of a monolithic implementation of the equivalent network of FIG. 13, taken to show the coplanar electrodes ~~M1 and M3~~ B40 mounted on upper ~~lower~~ surface 42 ~~44~~ for connection to other circuitry. ~~Although not visible from this view, it should be understood the electrodes~~ Electrodes M2, M4 and M5 are adjacent to the lower ~~upper~~ surface 44 ~~42~~ of the piezoelectric material 30 ~~and~~ electrodes MG1 and MG2 are also mounted to the lower surface 42. Electrodes MG1 and MG2 are combined into a single electrode. Alternatively, electrodes M1 and M3 may be mounted adjacent to the lower ~~upper~~ surface 44, with the positions of the other electrodes reversed accordingly, by changing the fabrication steps. If it is desired to have electrodes MG1 and MG2 on a surface opposing the electrodes M1 and M3, then resonators X2 and X3 are not decomposed and electrodes M4 and M5 are not added.

Insert B40

Sub C5

~~FIGS. 15A-D illustrate the process for~~ fabricating the series connected resonators of FIG. 13. FIG. 15A shows the first layer metalizations that form electrodes M1, M3 and signal ground (MG1 and MG2 combined). FIG. 15B shows the deposition of the piezoelectric material 30. ~~FIG. 15C~~ shows a second layer metalization that forms electrodes M2, M4 and M5 (MG1 and MG2 combined). FIG 15D is a schematic view showing the

PAGE 23

~~relative locations of the six resonators within the monolithic implementation of the pi network~~.

The optimizing method also covers networks such as L networks. FIG. 16 shows the topology of a conventional L-network within an electrical circuit. The L network comprises a series resonator X1 and a shunt element such as resonator X2. Electrode M1 of resonator X1 provides a lead for interconnecting the network to other circuitry such as resistor Rg to receive an input for the network. Similarly, electrode M2, which is shared by resonators X1 and X2, provides a lead for interconnecting the network to other circuitry such as resistor R_1 to provide an output for the network. Electrode MG completes resonator X2 and is a lead for interconnecting the network to signal ground.

FIG. 17 is a perspective ~~cross sectional~~ view of an implementation of the network of FIG. 16~~, taken so as to~~ show only resonator X1. It can be readily seen that the electrodes M1 and M2 are on opposing surfaces of the piezoelectric material 30. If both leads 38 and 40 are to be located on lower surface 44 of material 30, then lead 40 will have to be moved to lower surface 44. ~~bonded to discrete components, then lead 38 will have~~ to be connected to a bonding pad on the upper surface 42.

With the method of the invention, this connection is made by decomposing resonator X1 into series connected resonators X11 and X12 ~~X12 and X22~~, as shown in the schematic diagram of FIG. 18. This adds an additional electrode M3 on the ~~lower~~ upper ~~44~~ 42 ~~upper~~ surface ~~42~~. ~~If~~ it is desirable to have electrode MG

(signal ground) on the ~~lower~~ upper ~~upper~~ surface as well, then resonator X2 should be decomposed into series connected resonators X21 and X22, adding the additional floating electrode M4. The optimized L network thus comprises a first resonator such as X12 that includes a first electrode M3 for connection to other circuitry. A shunt element such as resonator X2 of FIG. 16 is connected to the resonator X12 at electrode M3. To add the additional electrode needed for connecting at upper surface 42, resonator X11 is series connected to resonator X12 at electrode M2. Resonators X11 and X12 are the only connections to electrode M2. The series connected resonators place electrode M1 on the same ~~lower~~ upper ~~upper~~ surface ~~42~~ 44 as electrode M3.

FIG. 19 is a perspective ~~cross sectional~~ view of a monolithic implementation of the equivalent network of FIG. 18, taken to show the coplanar electrodes M1 and M3 on upper ~~lower~~ surface 42 ~~44~~. ~~Although not completely visible from this view, it should be understood that electrode M2 and M4 are adjacent to the upper surface 42 of the piezoelectric material 30 and electrode MG is mounted to the lower surface 44~~. Alternatively, electrodes M1 and M3 may be mounted adjacent to the lower ~~upper~~ surface 44 ~~42~~, with the positions of the other electrodes reversed accordingly. If it is desired to have electrode MG on a surface opposing electrodes M1 and M3, then resonator X2 is not decomposed and electrode M4 is not added.

Ins C6 Sub C6

~~FIGS. 20A-D illustrate the process for~~ fabricating the series connected resonators of FIG. 19. FIG. 20A shows the first layer metalizations that form electrodes M1 and M3 and signal ground (electrode MG). FIG. 20B shows the deposition of the piezoelectric material 30. FIG. 20C shows a second layer metalization that forms electrodes M2 and M4 ~~M2, M3 and M5~~. FIG. 20D is a schematic view showing the relative locations of the four resonators within the monolithic implementation of the optimized L network.

a

The method is not limited, of course, to the basic resonator networks described above. It may be applied wherever it is desirable to place an electrode on a specific surface of the piezoelectric material for making a connection to other circuitry. The versatility of the method can be seen in optimizing the circuit of FIG. 21. The circuit shown is a T ladder network comprising a number of piezoelectric resonators and shunt elements that may also be piezoelectric resonators.

B

FIG. 22 is a cross sectional view of the ladder network of FIG. 21, ~~taken to show only the structure of~~ resonators X1, X2 and X3. It can be readily seen that the electrode M1 is adjacent to upper surface 42 and electrode M4 adjacent to lower surface 44 of the piezoelectric material 30. Consequently lead 38 of electrode M1 is exposed on the upper surface and lead 64 of electrode M4 is adjacent to ~~buried between~~ the piezoelectric material's lower

B3

26

surface 44 ~~and substrate 32~~. If electrode M4 is to be bonded to discrete components, then lead 64 must be connected to the upper surface 42.

With the method of the invention, this connection can be made by decomposing resonator X2 into series connected resonators X21 and X22, as shown in the schematic diagram of FIG. 23. This adds an additional electrode M5 on the upper surface 42, as shown in FIG. 24, with its own lead 70. Both leads 38 and 70, which connect the ladder network to other circuitry, are now in a position where such connection may be easily made. ~~Electrode MG (signal ground) is~~ B41 also on upper surface 42 for ease of connection.

FIGS. 25A-D illustrate the process for fabricating the series connected resonators of FIG. ~~20~~ 25. FIG. ~~20A~~ 25A shows the first layer metalizations that form electrodes ~~M1~~ M2 and ~~M2~~ M4. FIG. ~~20B~~ 25B shows the deposition of the piezoelectric material 30. FIG. ~~20C~~ 25C shows a second layer metalization that forms electrodes M1, M3, M5 and signal ground (electrode MG) 5, 1 and MG. FIG. ~~20D~~ 25D is a schematic view showing the relative locations of the six resonators within the monolithic implementation of the optimized T ladder network.

Similar implementations made be constructed for generalized pi and L ladder networks.

Having illustrated and described the principles of the invention in several preferred embodiments, it

should be apparent to those skilled in the art that the invention can be modified in arrangement and detail without departing from such principles. For example, these principles are readily applied to discrete implementations of piezoelectric-based resonator networks as well as monolithic implementations. I therefore claim all modifications coming within the spirit and scope of the following claims.

28